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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,231	02/19/2004	Lothar Benedict Moeller	Moeller 19-8	5230
46850	7590	12/23/2008	EXAMINER	
MENDELSON & ASSOCIATES, P.C. 1500 JOHN F. KENNEDY BLVD., SUITE 405 PHILADELPHIA, PA 19102			KIM, DAVID S	
			ART UNIT	PAPER NUMBER
			2613	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/782,231	MOELLER ET AL.	
	Examiner	Art Unit	
	DAVID S. KIM	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 06 October 2008.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,3,5-9,11,13-20 and 22-25 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1,3,5-9,11,13-20 and 22-25 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Withdrawal of Finality

1. A new ground(s) of rejection is made. Therefore, the previous rejection (mailed on 15 April 2008) has been withdrawn, and the finality of that rejection is withdrawn. Notice the details of the new ground of rejection below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Applicant has provided evidence in this file showing that the invention was owned by, or subject to an obligation of assignment to, the same entity as Moeller (U.S. Patent Application Publication No. US 2003/0170022 A1) at the time this invention was made, or was subject to a joint research agreement at the time this invention was made. However, reference Moeller additionally qualifies as prior art under another subsection of 35 U.S.C. 102, and therefore, is not disqualified as prior art under 35 U.S.C. 103(c).

Applicant may overcome the applied art either by a showing under 37 CFR 1.132 that the invention disclosed therein was derived from the invention of this application, and is therefore, not the invention "by another," or by antedating the applied art under 37 CFR 1.131.

5. **Claims 1, 3, 5, 7-9, 11, 14-20, and 23-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moeller, with reference to Singh (“Modulating Pulses in Long-Haul Optics Systems”), in view of Applicant's admitted prior art (hereinafter the “AAPA”), Engl et al. (U.S. Patent No. 7,173,993 B2, hereinafter “Engl”), and a concession by Applicant (hereinafter “CA”). Notice that Singh is applied according to the proper practice recognized by MPEP 2131.01, section III. That is, Singh is applied to show that a characteristic not disclosed in Moeller is inherent.

Regarding claim 1, Moeller, with reference to Singh, discloses:

A method of signal processing, comprising:

converting an optical signal having a duty cycle greater than one (Moeller, non-return-to-zero (NRZ) pulses in claim 9; Singh, NRZ pulses are “on for an entire period”, which is a duty cycle of one, and pulses generally undergo broadening in optical fiber, see Handling Impairments; thus, one would expect NRZ pulses received by Moeller to have a duty cycle greater than one) into an electrical signal having an amplitude corresponding to optical power of the optical signal (e.g., 230 in Fig. 2, 530 in Fig. 5);

sampling the electrical signal using two or more sampling windows contained within a time interval having a one-bit length (the multiple sampling points in Fig. 4 correspond to one bit slot) to generate two or more bit estimate values (multiple sampling points in Fig. 4), wherein sampling the electrical signal comprises:

sampling the electrical signal at a first sampling position to generate a first sampling result (the left sampling point in Fig. 4);

comparing the first sampling result with a first decision threshold value to generate a first bit estimate value (e.g., threshold in Fig. 4);

sampling the electrical signal at a second sampling position to generate a second sampling result (the right sampling point in Fig. 4); and

comparing the second sampling result with a second decision threshold value to generate a second bit estimate value (e.g., threshold in Fig. 4); and

applying a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5).

Moeller does not expressly disclose:

wherein sampling the electrical signal comprises:

integrating the electrical signal over a first sampling window to generate a first integration result;

comparing the first **integration** result with a first decision threshold value to generate a first bit estimate value;

integrating the electrical signal over a second sampling window to generate a second integration result; and

comparing the second **integration** result with a second decision threshold value to generate a second bit estimate value.

Regarding the “sampling **window**” limitations, notice that Moeller teaches “sampling points” (e.g., “sampling points” in Fig. 4). However, it is known in the art to represent sampling instants as having finite widths, as shown by Engl (notice the finite widths of sampling instants T2, T21, and T22 in Figs. 3, 4, and 6). In view of such an alternate depiction of sampling instants, it follows that one may obviously characterize the “sampling points” of Moeller as “sampling **windows**”.

Regarding the “**integrating...over a...sampling window**” and “**integration**” limitations, notice that Moeller teaches the general concept of “sampling” (e.g., “sampling” in Fig. 4). However, integration over a sampling window is a known technique in the art, as noted by the AAPA (Applicant’s specification, p. 4-5, bridging paragraph), as a suitable way to implement the more general concept of “sampling”. Accordingly, the limitations of “**Integrating...over a...sampling window**” and “**Integration**” would only provide an obvious variation.

Moeller does not expressly disclose:

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wherein applying the logical function comprises applying an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

Rather, Moeller discloses the application of an "OR" function (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5) logic circuitry. Still, Moeller does disclose the option of applying other alternative circuitry (paragraph [0020]). The usage of the "OR" function is to reduce the error probability for logical "1" values (paragraph [0027]). Logically speaking, an "AND" function is an "OR" function for "0" values. That is, a regular "OR" function outputs a "1" if any input is a "1". Similar in operation, a regular "AND" function outputs a "0" if any input is a "0". At the time the invention was made, it would have been obvious to one of ordinary skill in the art to notice that such similar operation is an obvious variation of the method of Moeller. One of ordinary skill in the art would have been motivated to employ an "AND" function for the similar reason of employing an "OR" function, i.e., to reduce the probability for a particular bit estimate value, e.g., "0" values.

In the field of logic processing, it is an extremely common and obvious practice to consider **inverse** scenarios since inverse scenarios provide **equivalent** functionality with **alternate logic values** (e.g., changing "one" values to "zero" values and vice versa). An inverse scenario to the example of Moeller-022 could be that of properly detecting a "zero" value, represented by a notch or "valley" between two neighboring "plateaus" of high value (e.g., invert Fig. 4 of Moeller-022 by simply turning it upside-down). Whereas the express example of Moeller-022 focuses on decreasing the error probability for "ones", an **inverse** scenario could focus on decreasing the error probability for "zeros". In view of such considerations, the OR logic function in the express example of Moeller-022 would provide the **equivalent** inventive functionality as that of an AND logic function in an **inverse** scenario. The rationale for using either logic function would be the **same**: to reduce the error probability for a particular bit estimate value, i.e., "one" values for the express example of Moeller-022 and "zero" values for an inverse scenario, resulting in improved performance for each respective scenario.

Moreover, Applicant appears to express the same opinion of obviousness of different scenarios in CA, i.e., the following concession from Applicant's own specification:

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The choice of logical function applied to the bit estimate values corresponding to sampling windows M1 and M2 is primarily determined by the type of error-causing impedance to the optical signal. For example, as already indicated above, for the eye diagram of Fig. 3A, most decoding errors are related to false binary "ones" attributed to waveform 304. In this situation, the "AND" function is an appropriate function choice because it returns a "0" whenever at least one of the bit estimate values is "0". In a different situation, e.g., when most decoding errors are related to false binary "zeros" attributed to waveform 302, the "OR" function would be an appropriate function choice. ***One skilled in the art will appreciate that, depending on the type of impedance and/or waveform shape, other logical functions or other numbers (e.g., three or more) of sampling windows may similarly be employed.*** For example, the present invention may be implemented with three sampling windows, wherein (i) an "OR" function is applied to the bit estimate values corresponding to two of these sampling windows and (ii) an "AND" function is applied to the bit estimate value corresponding to the third sampling window and the value returned by the "OR" function to produce the final bit value to be output from the decoder.

(Applicant's specification, p. 6, l. 17-30, emphasis Examiner's).

Applicant concedes that one skilled in the art will appreciate different variations, including "other logical functions", to address different scenarios, including different "type[s] of impediment[s] and/or waveform shape[s]". Such sentiments are within the spirit of Moeller-022's broad range of considerations of improving jitter tolerance, as noted above. Applicant even notes the **same** specific scenario employed by Moeller-022, i.e., the "OR" function to address false binary "zeros". As Applicant concedes that one skilled in the art will appreciate different variations, in view of Applicant's variation of employing an "OR" function to address false binary "zeros", it similarly follows that one skilled in the art will appreciate different variations, in view of Moeller-022's **same** variation of employing an "OR" function to address false binary "zeros".

Accordingly, this obviousness argument addresses the particular and obvious variation of considering an **inverse** scenario (i.e., employing an "AND" function to address false binary "ones"), which provides **equivalent** functionality with **alternate logic values**, as is common and obvious in the field of logic processing.

Regarding claim 3, Moeller in view of the discussion above (hereinafter the "DA") discloses:

The method of claim 1, wherein:

each sampling window has a width (Engl. notice the finite widths of sampling instants T2, T21, and T22 in Figs. 3, 4, and 6; AAPA, "width" on p. 4-5, bridging paragraph);

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the electrical signal has a series of waveforms comprising first and second pluralities of waveforms, wherein each waveform of the first plurality represents a binary "0" and each waveform of the second plurality represents a binary "1" (waveforms below the threshold represent "0", waveforms above the threshold represent "1"); and

for each sampling window:

a waveform is integrated over the sampling window width to generate a corresponding bit estimate value (AAPA, "integration" on p. 4-5, bridging paragraph); and

the sampling window width is selected to reduce contribution of the second plurality of waveforms into integration results corresponding to the first plurality of waveforms (e.g., suggested by the narrow widths of T21, T2, and T22 in Fig. 6 of Engl, i.e., no contribution from jitter of adjacent waveforms into the sampling windows of T21, T2, and T22).

Regarding claim 5, Moeller in view of the DA does not expressly disclose:

The method of claim 1, wherein the first decision threshold value is different from the second decision threshold value.

However, setting different threshold values is an obvious practice for the method of Moeller. One of ordinary skill in the art would have been motivated to do this to provide design flexibility in addressing various sources of noise in decision circuit 240, with consideration of timing jitter. For example, lower threshold values may help avoid spontaneous beat noise at the mark level of a sampling window, and higher threshold values may help avoid spontaneous beat noise and thermal noise at the space level of a sampling window. Employing different threshold values at different sampling points allows one to vary the influence of these various sources of noises at different sampling points, thus providing a practitioner with the ability to tailor the operation of decision circuit 240 for various bit patterns.

Regarding claim 7, Moeller in view of the DA discloses:

The method of claim 1, comprising:

generating a first clock signal based on the electrical signal (10 GHz clock tone in paragraph [0021]);

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multiplying a frequency of the first clock signal to generate a second clock signal (40 GHz clock from 1:4 frequency multiplier in paragraph [0021]); and

sampling the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying the first and second bit estimate values (sampling according to the 40 GHz clock in paragraph [0021]).

Regarding claim 8, Moeller in view of the DA discloses:

The method of claim 7, comprising:

separating the first and second bit estimate values from the bit stream while discarding all other bits of the bit stream (demultiplexer 250 in Fig. 2).

Regarding claim 9, Moeller in view of the DA discloses:

The method of claim 1, comprising:

generating a clock signal based on the electrical signal (40 GHz clock from 1:4 frequency multiplier in paragraph [0021]);

sampling first and second copies of the electrical signal at a sampling rate corresponding to the clock signal (sampling according to the 40 GHz clock in paragraph [0021]), wherein:

the first copy is sampled to generate the first bit estimate value (values of top input to gate 260 in Fig. 2);

the second copy is sampled to generate the second bit estimate value (values of bottom input to gate 260 in Fig. 2); and

the first and second copies are sampled with a relative time delay (delay 280 in Fig. 2).

Regarding claim 11, Moeller in view of the DA discloses:

An optical receiver, comprising:

a signal converter adapted to convert an optical signal having a duty cycle greater than one (Moeller, non-return-to-zero (NRZ) pulses in claim 9; Singh, NRZ pulses are “on for an entire period”, which is a duty cycle of one, and pulses generally undergo broadening in optical fiber, see Handling Impairments; thus, one would expect NRZ pulses received by Moeller to have a duty cycle greater than

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one) into an electrical signal having an amplitude corresponding to optical power of the optical signal (e.g., 230 in Fig. 2, 530 in Fig. 5); and

a decoder coupled to the signal converter and adapted to:

(i) sample the electrical signal using two or more sampling windows contained within a time interval having a one-bit length (the multiple sampling points in Fig. 4 correspond to one bit slot; Engl, notice the finite widths of sampling instants, “windows”, T2, T21, and T22 in Figs. 3, 4, and 6) to generate two or more bit estimate values (multiple sampling points in Fig. 4);

(ii) apply a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5);

(iii) integrate the electrical signal over a first sampling window to generate a first integration result (the left sampling point in Fig. 4; Engl, “windows” of T2, T21, and T22 in Figs. 3, 4, and 6; AAPA, “integration” on p. 4-5, bridging paragraph);

(iv) compare the first integration result with a first decision threshold value to generate a first bit estimate value (e.g., threshold in Fig. 4);

(v) integrate the electrical signal over a second sampling window to generate a second integration result (the right sampling point in Fig. 4; Engl, “windows” of T2, T21, and T22 in Figs. 3, 4, and 6; AAPA, “integration” on p. 4-5, bridging paragraph); and

(vi) compare the second integration result with a second decision threshold value to generate a second bit estimate value (e.g., threshold in Fig. 4).

Moeller does not expressly disclose:

wherein the decoder comprises an “AND” gate adapted to apply an “AND” function to the first and second bit estimate values to generate a bit of the bit sequence.

Rather, Moeller discloses the application of an “OR” function (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5) logic circuitry. Still, Moeller does disclose the option of applying other alternative circuitry (paragraph [0020]). The usage of the “OR” function is to reduce the error probability for logical “1” values (paragraph [0027]). Logically speaking, an “AND” function is an “OR” function for “0” values. That is, a

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regular "OR" function outputs a "1" if any input is a "1". Similar in operation, a regular "AND" function outputs a "0" if any input is a "0". At the time the invention was made, it would have been obvious to one of ordinary skill in the art to notice that such similar operation is an obvious variation of the apparatus of Moeller. One of ordinary skill in the art would have been motivated to employ an "AND" function for the similar reason of employing an "OR" function, i.e., to reduce the probability for a particular bit estimate value, e.g., "0" values.

In the field of logic processing, it is an extremely common and obvious practice to consider **inverse** scenarios since inverse scenarios provide **equivalent** functionality with **alternate logic values** (e.g., changing "one" values to "zero" values and vice versa). An inverse scenario to the example of Moeller-022 could be that of properly detecting a "zero" value, represented by a notch or "valley" between two neighboring "plateaus" of high value (e.g., invert Fig. 4 of Moeller-022 by simply turning it upside-down). Whereas the express example of Moeller-022 focuses on decreasing the error probability for "ones", an **inverse** scenario could focus on decreasing the error probability for "zeros". In view of such considerations, the OR logic function in the express example of Moeller-022 would provide the **equivalent** inventive functionality as that of an AND logic function in an **inverse** scenario. The rationale for using either logic function would be the **same**: to reduce the error probability for a particular bit estimate value, i.e., "one" values for the express example of Moeller-022 and "zero" values for an inverse scenario, resulting in improved performance for each respective scenario.

Moreover, Applicant appears to express the same opinion of obviousness of different scenarios in CA, i.e., the following concession from Applicant's own specification:

The choice of logical function applied to the bit estimate values corresponding to sampling windows M1 and M2 is primarily determined by the type of error-causing impediment to the optical signal. For example, as already indicated above, for the eye diagram of Fig. 3A, most decoding errors are related to false binary "ones" attributed to waveform 304. In this situation, the "AND" function is an appropriate function choice because it returns a "0" whenever at least one of the bit estimate values is "0". In a different situation, e.g., when most decoding errors are related to false binary "zeros" attributed to waveform 302, the "OR" function would be an appropriate function choice. ***One skilled in the art will appreciate that, depending on the type of impediment and/or waveform shape, other logical functions or other numbers (e.g., three or more) of sampling windows may similarly be employed.*** For example, the present invention may be implemented with three sampling windows, wherein (i) an "OR" function is applied to the bit estimate values corresponding to two of these sampling windows and (ii) an "AND" function is applied to the bit estimate value corresponding to the third sampling window

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and the value returned by the "OR" function to produce the final bit value to be output from the decoder.

(Applicant's specification, p. 6, l. 17-30, emphasis Examiner's).

Applicant concedes that one skilled in the art will appreciate different variations, including "other logical functions", to address different scenarios, including different "type[s] of impediment[s] and/or waveform shape[s]". Such sentiments are within the spirit of Moeller-022's broad range of considerations of improving jitter tolerance, as noted above. Applicant even notes the **same** specific scenario employed by Moeller-022, i.e., the "OR" function to address false binary "zeros". As Applicant concedes that one skilled in the art will appreciate different variations, in view of Applicant's variation of employing an "OR" function to address false binary "zeros", it similarly follows that one skilled in the art will appreciate different variations, in view of Moeller-022's **same** variation of employing an "OR" function to address false binary "zeros".

Accordingly, this obviousness argument addresses the particular and obvious variation of considering an **inverse** scenario (i.e., employing an "AND" function to address false binary "ones"), which provides **equivalent** functionality with **alternate logic values**, as is common and obvious in the field of logic processing.

Regarding claim 14, Moeller in view of the DA discloses:

The receiver of claim 11, comprising:

a decision circuit (e.g., decision circuit 240 in Fig. 2) coupled to the signal converter;
a clock recovery circuit coupled to the signal converter and adapted to generate a first clock signal based on the electrical signal (implied circuitry for recovering the 10 GHz clock tone in paragraph [0021]); and

a clock multiplier coupled between the clock recovery circuit and the decision circuit and adapted to multiply a frequency of the first clock signal to generate a second clock signal (40 GHz clock from 1:4 frequency multiplier in paragraph [0021]), wherein the decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying first and second bit estimate values (sampling according to the 40 GHz clock in paragraph [0021]).

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Regarding claim 15, Moeller in view of the DA discloses:

The receiver of claim 14, comprising:

a de-multiplexer (250 in Fig. 2) having an input port and a plurality of output ports, wherein:

the input port is coupled to the decision circuit (240 in Fig. 2);

a first output port is adapted to receive a signal corresponding to the first bit estimate value (top output port to gate 260); and

a second output port is adapted to receive a signal corresponding to the second bit estimate value (bottom output port to gate 260), wherein the "AND" gate is coupled to the first and second output ports (see the treatment of claim 11 above regarding this "AND" gate limitation).

Regarding claim 16, Moeller in view of the DA discloses:

The receiver of claim 11, comprising:

first and second decision circuits (560₁ and 560₂ in Fig. 5), each coupled to the signal converter;

a clock recovery circuit (10 Gb/s Clk) coupled between the signal converter and the first and second decision circuits and adapted to generate a clock signal based on the electrical signal, wherein:

each decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the clock signal (sampling in paragraph [0034]);

the first decision circuit is adapted to generate the first bit estimate value (e.g., 560₁ in Fig. 5);

the second decision circuit is adapted to generate the second bit estimate value (e.g., 560₂ in Fig. 5); and

the first and second decision circuits sample the electrical signal with a relative time delay (time delay in Fig. 5).

Regarding claim 17, Moeller in view of the DA discloses:

The receiver of claim 16, wherein the "AND" gate is coupled to the first and second decision circuits (see the treatment of claim 11 above regarding this "AND" gate limitation).

Regarding claim 18, Moeller in view of the DA discloses:

The receiver of claim 16, wherein each decision circuit is adapted to:

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integrate the electrical signal over a respective sampling window to generate a respective integration result; and

compare the respective integration result with a respective decision threshold value to generate a bit estimate value (AAPA, “integration” on p. 4-5, bridging paragraph, to generate a respective integration result for comparison with a respective decision threshold of Fig. 4 of Moeller to generate the output bit estimate values).

Regarding claim 19, Moeller, with reference to Singh, does not expressly disclose:

The receiver of claim 18, wherein the first and second decision circuits use different decision threshold values.

Claim 5 introduces a similar limitation. An obviousness argument is applied to address this similar limitation in the treatment of claim 5 above. Similarly, the same obviousness argument is applied here to address this corresponding limitation in claim 19.

Regarding claims 20 and 23-25, claims 20, 23, 24, and 25 are system claims that introduce limitations that correspond to the limitations introduced by receiver claims 11, 15, 17, and 19, respectively. Therefore, the recited means in receiver claims 11, 15, 17, and 19 read on the corresponding means in system claims 20 and 23-25.

6. **Claims 6, 13, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moeller in view of the DA, as applied to the claims above, and further in view of Yonenaga et al. (“Dispersion-tolerant optical transmission system using duobinary transmitter and binary receiver”, hereinafter “Yonenaga”).

Regarding claim 6, Moeller in view of the DA does not expressly disclose:

The method of claim 1, wherein the optical signal is an optical duobinary signal.

Although Moeller considers return-to-zero (RZ) coding and NRZ coding (paragraph [0017] and claim 9), notice the duobinary coding of Yonenaga (p. 1530, col. 2, middle paragraph – p. 1531, 1st paragraph). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to employ the duobinary coding of Yonenaga. One of ordinary skill in the art would have been motivated to do this for any of the following advantages: higher tolerance to fiber chromatic dispersion

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that limits transmission distance and suppression of stimulated Brillouin scattering (SBS) (Yonenaga, p. 1530-1531, bridging paragraph).

Regarding claim 13, Moeller in view of the DA and Yonenaga discloses:

The receiver of claim 11, wherein the optical signal is an optical duobinary signal (Yonenaga, p. 1530, col. 2, middle paragraph – p. 1531, 1st paragraph).

Regarding claim 22, Moeller in view of the DA and Yonenaga discloses:

The system of claim 20, wherein the optical signal is an optical duobinary signal (Yonenaga, p. 1530, col. 2, middle paragraph – p. 1531, 1st paragraph).

Response to Arguments

7. Applicant's arguments filed in the Appeal Brief on 06 October 2008 have been considered.

Applicant's presents five sets of arguments. The first set is moot. The second through fifth sets are not persuasive.

Regarding the first set of arguments, Applicant presents points about the "Steps of Integrating" ("Steps of Integrating" on p. 5-9). These points are moot in view of the new ground of rejection based on information from the AAPA, Engl, and the CA.

Regarding the second set of arguments, Applicant presents one salient point about the "Duty Cycle Greater than One" ("Duty Cycle Greater than One" on p. 9-11).

Regarding the first point, Applicant states:

On page 5 of the advisory action dated 07/21/2008, the Examiner attempts to counter these arguments by stating that:

Moeller-022 **already** positively teaches the use of an NRZ signal (Moeller-022, claim 9). Singh... shows that pulses generally undergo broadening in optical fiber... Accordingly, **without** any consideration of obviousness, one would expect the NRZ signal of Moeller-022 to experience pulse broadening, which would result in a duty cycle greater than one.

In response, the Appellants submit that the Examiner cannot possibly make an obviousness-type rejection and, at the same time, take "any consideration of obviousness" out of the picture. If the Examiner wanted to make a rejection "**without** any consideration of obviousness," then he should have made a rejection under 35 U.S.C. § 102, and not under 35 U.S.C. § 103(a), which, of course, he could not properly do. It appears that, with respect to the

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"duty cycle" limitation, the Examiner conveniently chose to disregard the familiar framework set forth in Graham v. John Deere Co. and subsequently clarified in KSR International Co. v. Teleflex Inc. The Appellants submit that, due to the evident deviation from the proper examination guidelines, the part of the rejection directed at the "duty cycle" limitation must fall for want of proper methodology.

(Appeal Brief, end of p. 10 – p. 11, first full paragraph).

Examiner respectfully notes that Singh is applied according to the proper practice recognized by MPEP 2131.01, section III. That is, Singh is applied to show that a characteristic not disclosed in Moeller is inherent. Such an application of Singh does not require a determination of obviousness. Accordingly, this point is not persuasive, and Applicant's second set of arguments is not persuasive.

Regarding the third set of arguments, Applicant presents two salient points about the "Step of Applying an AND Function" ("Step of Applying an AND Function" on p. 11-14).

Regarding the first point, Applicant states:

On page 7 of the advisory action dated 07/21/2008, the Examiner attempts to counter these arguments by stating that "claim 1 of Moeller-022 suggests a **broader** use of logic ... as no mention of an OR gate appears in the claims until claim 11."

In response, the Appellants submit that what the Examiner is trying to do here is to substitute the inquiries mandated by Graham v. John Deere Co. and KSR International Co. v. Teleflex Inc. by an irrelevant inquiry into which claim or concept is broader. The latter inquiry might be relevant to infringement analyses, but it is utterly improper to use this inquiry instead of the requisite obviousness-determination inquiries. As an example, it is a well-recognized fact in patent law that an invention defined by a narrower claim can infringe a broader claim and, at the same time, the narrower claim can still be non-obvious over the broader claim.

(Appeal Brief, p. 13, third and fourth paragraphs).

Examiner respectfully notes that any "requisite obviousness-determination inquiries" must first be **preceded** by a clear and established understanding of the scope of teachings actually disclosed, implied, and suggested by the prior art. Thus, it is very relevant to understand the context of any prior art of record in any "requisite obviousness-determination inquiries". In the instant case, there must be a clear and established understanding of the scope of teachings actually disclosed, implied, and suggested by Moeller-022. Both Applicant and Examiner point to the following portion of Moeller-022 to argue different interpretations and conclusions:

Although the front-end pre-amplified receiver 200 of FIG. 2 is depicted as a relatively complex receiver, a less complex conventional front-end pre-amplified receiver can also be implemented

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within various embodiments of the present invention. Additionally, although the logic circuitry 260 of FIG. 2 is depicted as an OR logic gate, other circuitry or devices that are able to determine a resulting logic state of at least one input signal can be implemented with the concepts of the present invention (Moeller-022, paragraph [0020]).

In short, Applicant interprets this portion as **exclusively** teaching the use of “an OR logic gate”. Examiner notes that the actual text of this portion is **not so narrow** and interprets this portion, along with other portions of Moeller-022, as supporting other logic functions besides that of an OR logic function.

According to Applicant’s interpretation of Moeller-022, Moeller-022 is closed to the idea of applying a different logic function, i.e., a logic function other than an OR logic function, in an obviousness determination. According to Examiner’s interpretation of Moeller-022, Moeller-022 is open to the idea of applying a different logic function, i.e., a logic function other than an OR logic function, in an obviousness determination. Therefore, **before** one attempts any “requisite obviousness-determination inquiries”, there must be a clear and established understanding of the scope of teachings actually disclosed, implied, and suggested by Moeller-022. Otherwise, there may be contradictory interpretations and conclusions, as evidenced by the contradictory positions of Applicant and Examiner. Accordingly, this first point is not persuasive.

Regarding the second point, Applicant states:

On page 8 of the advisory action, the Examiner also attempts to present an alternative interpretation of the above-quoted portion of Moeller-022’s paragraph [0020], which interpretation is different from that presented above by the Appellants. More specifically, the Examiner emphasizes the following phrases in Moeller-022’s paragraph [0020]: “to determine a resulting logic state” and “with the concepts of the present invention.” Serial No. 10/782,231 - 13- Moeller 19-8 (990.0519)

In response, the Appellants would like to stress that a logic state has no meaning by itself and is always determined with reference to the corresponding logic function. Indeed, the same two input signals can result in one logic state when used as inputs to a first logic function, and in a completely different logic state when used as inputs to a different second logic function. Since Moeller-022’s paragraph [0020] only mentions “an OR logic gate,” it follows that the phrases emphasized by the Examiner talk about the logic states of the OR function, and not of an arbitrary logic function, as the Examiner suggests.

(Appeal Brief, p. 13, last paragraph – p. 14, first paragraph).

Clearly, Applicant and Examiner hold different interpretations of the scope of teachings actually disclosed, implied, and suggested by Moeller-022. Applicant relies largely on (A) only one portion of Moeller-022 (paragraph [0020]) to reach a conclusion. Examiner relies on the (A) same portion of Moeller-022

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(paragraph [0020]) and (B) other portions of Moeller-022 (paragraph [0017], claims 1 and 11 of Moeller-022).

Applicant relies on (A) Moeller-022's paragraph [0020] to conclude that Moeller-022 application of an OR logic function is exclusive of other logic functions.

Examiner also relies on (A) Moeller-022's paragraph [0020]:

Although the front-end pre-amplified receiver 200 of FIG. 2 is depicted as a relatively complex receiver, a less complex conventional front-end pre-amplified receiver can also be implemented within various embodiments of the present invention. Additionally, although the logic circuitry 260 of FIG. 2 is depicted as an OR logic gate, *other circuitry or devices that are able to determine a resulting logic state of at least one input signal can be implemented with the concepts of the present invention* (Moeller-022, paragraph [0020], emphasis Examiner's).

Applicant reads the highlighted portion as “the logic states of the OR function, and not of an arbitrary logic function” (Appeal Brief, p. 14, first paragraph). However, the actual text is not so *narrow*. Rather, the text states, “*other circuitry or devices that are able to determine a resulting logic state of at least one input signal can be implemented with the concepts of the present invention*”. “[T]o determine a resulting logic state” is broader than Applicant’s reading of “the logic states of the OR function, and not of an arbitrary logic function”. Accordingly, Moeller-022 is open to the idea of applying a different logic function, i.e., a logic function other than an OR logic function, in an obviousness determination.

Examiner also relies on (B) other portions of Moeller-022.

- Consider paragraph [0017]. Examiner respectfully notes that the scope of the invention of Moeller-022 is **broad**er than the specific examples provided (e.g., Fig. 4). For example, paragraph [0017] states that "the inventive concept can be advantageously implemented in various other transmission systems wherein it is desirable to improve a jitter tolerance".

When paragraph [0020] cites the “concepts of the present invention”, as noted above, the “concepts of the present invention” address the **broad**er issue of jitter tolerance, not just the **specific** example of Fig. 4 of Moeller-022 employing the OR gate of Fig. 2 of Moeller-022.

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- Consider claims 1 and 11. Examiner respectfully notes that claim 1 of Moeller-022 suggests a **broader** use of logic as the invention of Moeller-022 as no mention of an OR gate appears in the claims until dependent claim 11 of Moeller-022. Although an OR logic function is expressly disclosed, the contextual principles of Moeller-022 do not appear to exclusively limit the logic function to that of an OR logic function.

In view of the more comprehensive consideration of additional portions of Moeller-022, noted as (A) and (B) above, Examiner concludes that Moeller-022 is open to the idea of applying a different logic function, i.e., a logic function **other than** an OR logic function, in an obviousness determination. Applicant's less comprehensive consideration of only a small portion of Moeller-022, noted as (A) above, is less persuasive. Accordingly, Applicant's second point is not persuasive.

As an additional note, Examiner does not mean to conclude that Moeller-022 positively teaches or suggests the application of an AND logic function. The standing rejection clearly relies on additional considerations of the state of art, outside of Moeller-022, to show that the application of an AND logic function would be an obvious variation.

Summarily, Applicant's third set of arguments is not persuasive.

Regarding the fourth set of arguments, Applicant presents one salient point about the "Combination of Features" ("Combination of Features" on p. 14-15).

Regarding the first point, Applicant states:

Even if each of the three above-discussed limitations of claim 1 were obvious over Moeller- 022 and Singh, which the Appellants do not admit, the Appellants submit that the combination of the corresponding features would still be non-obvious.

In particular, the Appellants would like to point out that the three above-discussed features have a positive synergistic effect on the performance of the optical receiver. For example, the steps of integrating help to smooth out the optical spikes produced by photon bursts generated by spontaneous beat noise and/or thermal noise (see, e.g., Appellants' Fig. 3B). The step of applying the logical "AND" function then further guards against a decoding error when such an optical spike is so large as to still cause one of the smoothed-out samples in a "zero" bit interval to overshoot the decision threshold. As already indicated above, integrating the signal and applying the "AND" function to the signal samples is particularly beneficial for signals having

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a duty cycle greater than one because decoding errors for such signals are dominated by the errors in the "zero" bit intervals. Thus, claim 1 defines a robust signal processing scheme that is significantly more advantageous than a processing scheme utilizing each of the above-discussed features separately, rather than all three of them together as required by claim 1 (see, e.g., Appellants, Figs. 7 and 8A-B and the corresponding description).

For all these reasons, the Appellants submit that claim 1 is non-obvious over the cited art and that the rejection of claim 1 should be withdrawn. For similar reasons, it is submitted that claims 11 and 20 are allowable over the cited references. Since claims 3, 5-9, 13-19, and 22-25 depend variously from claims 1, 11, and 20, it is further submitted that those claims are allowable over the cited references. The Appellant submits therefore that the rejections of claims 1, 3, 5-9, 11, 13-20, and 22-25 under § 103 have been overcome.

(Appeal Brief, p. 14, third paragraph – p. 15, first paragraph).

Examiner respectfully notes that one would expect similar effects from the combination of the standing rejection.

Regarding "the steps of integrating help to smooth out the optical spikes produced by photon bursts generated by spontaneous beat noise and/or thermal noise", notice the same type of integrating, exemplified by the AAPA ("integration" on p. 4-5, bridging paragraph).

Regarding the "step of applying the logical 'AND' function then further guards against a decoding error when such an optical spike is so large as to still cause one of the smoothed-out samples in a 'zero' bit interval to overshoot the decision threshold", notice the same benefit of employing an "AND" function to address false binary "ones" where the bit interval should be a "zero" bit interval, as addressed by the obviousness argument in the treatment of claim 1 above. More exactly, the obviousness argument in the treatment of claim recognizes that, in the field of logic processing, it is an extremely common and obvious practice to consider **inverse** scenarios since inverse scenarios provide **equivalent** functionality with **alternate logic values**.

Regarding the "signals having a duty cycle greater than one", notice the same type of signals, exemplified by Moeller and Singh (Moeller, non-return-to-zero (NRZ) pulses in claim 9; Singh, NRZ pulses are "on for an entire period", which is a duty cycle of one, and pulses generally undergo broadening in optical fiber, see Handling Impairments; thus, one would expect NRZ pulses received by Moeller to have a duty cycle greater than one).

Accordingly, this point is not persuasive, and Applicant's fourth set of arguments is not persuasive.

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Regarding the fifth set of arguments, Applicant presents one salient point about the rejections of claim 6 and 13 (p. 15).

Regarding the first point, Applicant states:

The Appellants further direct the Board's attention to the following facts. On page 8 of the advisory action dated 07/21/2008, the Examiner admitted that "the standing rejection [of claim 1] relies on an **NRZ signal** (NRZ pulses in claim 9 of Moeller-022)." However, a duobinary signal is an **inherently return-to-zero (RZ) signal**. Yet, claim 6 is rejected "as being unpatentable over Moeller, with reference to Singh, **as applied to the claims** above" (emphasis added; see paragraph 5 of the final office action dated 04/15/2008).

The Appellants submit that the rejection of claim 6 is improper because the rejection rationale applied by the Examiner to the base claim is only applicable to an NRZ signal and, without more, is not automatically extendible to an RZ signal, such as a duobinary signal.

(Appeal Brief, middle of p. 15 – end of p. 15).

Examiner respectfully directs attention to Yonenaga and supplemental teachings of prior art, Weik (*Fiber Optics Standard Dictionary*, 3rd ed.) and Franck et al. (U.S. Patent No. 6,188,497 B1, hereinafter "Franck").

Yonenaga shows that an optical duobinary signal (Fig. 1(c)) and an NRZ waveform (Fig. 1(a), NRZ on p. 1532, col. 1, last paragraph) may have the same waveform (notice the similar waveforms in Figs. 1(a) and 1(c)). Therefore, a duobinary signal is not inherently an RZ signal.

Weik teaches that an RZ signal is characterized as "a signal that reverts to zero **during** each bit interval, such as return to the zero between each bit even in a series of consecutive 1s, i.e., mark conditions" ("return to zero" on p. 873). The optical duobinary signal of Yonenaga (Fig. 1(c)) does not exhibit these characteristics. Therefore, a duobinary signal is not inherently an RZ signal.

Franck teaches an example of a duobinary signal and labels it as "NRZ duo-binary" (col. 7, l. 18). Therefore, a duobinary signal is not inherently an RZ signal.

Accordingly, this point is not persuasive, and Applicant's fifth set of arguments is not persuasive.

Summarily, Applicant's arguments are either moot or unpersuasive. Accordingly, Examiner respectfully maintains the standing rejections.

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Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID S. KIM whose telephone number is (571)272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth N. Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. S. K./
Examiner, Art Unit 2613

/Kenneth N Vanderpuye/
Supervisory Patent Examiner, Art Unit 2613